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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/756,901
Filing Date	January 14, 2004
First Named Inventor	Farrar, Paul
Group Art Unit	2823
Examiner Name	Clark, Sheila

Sheet 1 of 1

Attorney Docket No: 303.572US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>ML</i>		BOHR, M. , "Interconnect scaling-the real limiter to high performance ULSI", <u>International Electron Devices Meeting, IEEE, (1995),pp. 241-244</u>	
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EXAMINER

DATE CONSIDERED

2/19/07

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached